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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
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| EXAMINER | |
|---|---|
| ART UNIT | PAPER NUMBER |
| | |

DATE MAILED:

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

1- File Copy

| Office Action Summary | Application No. 09/316,697 | Applicant(s) Zhang |
|---|---|---|
| | Examiner MIKE QI | Group Art Unit 2871 |

☐ Responsive to communication(s) filed on _____

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

**Disposition of Claim**

☒ Claim(s) 1-23 is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-23 is/are rejected.

☐ Claim(s) _____ is/are objected to

☐ Claims _____ are subject to restriction or election requirement.

**Application Papers**

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

*--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---*

## DETAILED ACTION

### *Double Patenting*

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-23 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of U.S. Patent No. 5,995,189. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims 1-23 of this application using slight difference wording and that was obvious.

The claims of this application using wording "pixel portion" instead of the wording "matrix circuit" in the US 5,995,189. In fact, the "pixel portion" is the same thing as the "matrix circuit". The element 102 calls "matrix circuit" or "pixel section" (see specification of US 5,955,189 in column 5, line 13 and column 6, line 29). The wording "electro-optical display" and "liquid crystal display" are essentially the same thing also.

Therefore, claims 1-23 are met under double patenting rejection.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-23, the "pixel portion" is not a well defined as we don't know what applicant intends to include in this language.

For example, claim 2, the pixel portion according to the claim 1 including a plurality of thin film transistors and a peripheral drive circuit portion for driving the pixel portion. So that the pixel portion includes many components and may be various materials. Thus, how the substrate interval correction means (conductive films) can be a same material as the pixel portion?

Claim 16, "said first conductive layer is substantially equal to a pitch of said pixel electrode" is not clear. What is a layer that is equal to a pitch?

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 6, 18; 2-4, 8-10, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,200,847 (Mawatari et al) in view of US 5,619,358 (Tanaka et al).

Claims 1, 6 and 18, Mawatari et al discloses (col. 5, line 55 - col. 8, line 55 and Figs. 3 and 4) a structure of a liquid crystal display comprising:

a pair of substrates (101, 102);

a pixel portion including TFTs (106), signal lines (105), scanning lines (104) disposed in a matrix;

a driving circuit portion (120, 121) for driving the pixel portion;

a sealing member 103 for bonding the pair of substrates together.

Mawatari et al does not disclose expressly the substrate interval correction means disposed in a sealing forming region includes a conductive layer or first and second conductive layer not connected to any one of the pixel portion and the peripheral drive circuit portion.

However, Tanaka et al discloses (col. 4 line 50 - col.10 line 40 and Figs 1-11) a liquid crystal display having dummy electrodes 27a, 27b composed of first and second conductive films 25, 26.

The first conductive film 25 is formed at the end portions of the substrate 21 and 22, so as to extend from the regions of the substrate 21 and 22 where the sealing member 29 contacts with the substrate members 52 and 53 toward the side of the liquid crystal layer 54.

The second conductive film 26 is formed at the end portions of the substrate 21 and 22 and not being electrically connected to any one of any electrodes (see Fig. 1), so as to extend

from the regions of the substrate 21 and 22 where the sealing member 29 contacts with the substrate members 52 and 53 toward the outside of the substrates 21 and 22.

Such that the moisture coming from the atmosphere does not affect the liquid crystal layer, so as to prevent the corrosion. In addition, since the first and the second conductive film are disposed in the contacting region, the thickness of the liquid crystal layer near the sealing member is uniform, and the display quality is enhanced.

That is the motivation of the substrate interval correction means includes conductive layer not being electrically connected to any one of the pixel portion and the peripheral drive circuit portion.

Therefore, the substrate interval correction means to keep the substrate interval uniform and enhance the display quality as claimed in claims 1, 6 and 18 would have been obvious.

Claim 2, Tanaka et al discloses (col. 9 lines 28-45) the electrode film are realized by ITO or the like and processed to form plural signal electrode 23 and plural scanning electrode 24, etc. The substrate interval correction means conventionally employ the same material used in the other parts of the display, such as the ITO and bus metalizations and insulators for the benefit of avoiding the use of additional unnecessary layers. Therefore, the substrate correction means using same material as the other parts would have been obvious.

Claims 3-4 and 10, the pixel portion includes TFTs that consists of drain, source and gate electrodes need to be insulated each other, and that was conventional. In order to keep the same thickness of the liquid crystal layer the substrate interval correction means (conductive film)

should have a same structure as the pixel portion, so as to have same laminated structure and the same thickness to attain an even color display. Therefore, to arrange the interval correction conductive film has a same thickness and a same laminated structure as the pixel portion would have been obvious.

Claims 8, 9, 22 and 23 Tanaka et al discloses in Fig.1 an end surface of the first conductive layer 25 of the substrate interval correction means is not superimposed on an end surface of the second conductive layer 26, and the substrate interval correction means (conductive layer) has a same laminated structure as the pixel portion, and the signal lines 23 are superimposed on the scanning lines 24, so as to keep a uniform thickness of the liquid crystal layer near the sealing member, and the display quality is enhanced.

Also, Tanaka et al discloses in Fig.1 the conductive layer 26 is disposed along an edge portion of the substrate 52 and the branches are partially formed in an outer portion of the sealing region.

Therefore, the limitations as claimed in claims 8, 9, 22 and 23 would have been obvious.

7. Claims 5, 7, 11-14 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mawatari et al and Tanaka et al as applied to claims 1, 6 and 18 above, and further in view of US 5,148,301 (Sawatsubashi et al).

Claim 5, 7 and 19 Sawatsbashi et al discloses (col.6, lines 1-21) the driving circuit (112, 113) are disposed within the region of seal member 108 that the structure renders a miniaturizing of the liquid crystal display device, and shortens the length of the gate lines, the drain lines, so as

to reduce the wiring resistances and thus lower the potential drops of the gate lines. This enables the display device to exhibit a uniform display over the whole display region. That is the motivation to arrange the driving circuit disposed between the pixel portion and the sealing material. Therefore, a peripheral circuit for driving the pixel portion as claimed in claim 5, 7 and 19 would have been obvious.

Claims 11-13 and 20-21, Sawatsubashi et al discloses (col. 6 lines 23-41) the driving circuit 112 and 113 are disposed outside of the display region that means outside of the sealing forming region. Since the seal member 108 is directly fixed to the substrate 101 and 102, the adhesive force is rendered large, thereby firmly connected together by means of the sealing member 108 so that no defects appear in the driving circuit due to the stresses, so as to achieve an improved display quality. Therefore, to arrange an external circuit formed outside the sealing region as claimed in claims 11-13 and 20-21 would have been obvious.

Claim 14, the conductive layer comprises a plurality of linear wiring that is an inherent results, and would have been obvious.

8. Claims 15-17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mawatari et al and Tanaka et al as applied to claims 1, 6 and 18 above, and further in view of US 5,691,793 (Watanabe et al).

Claim 15, Watanabe et al discloses (col.11, lines 7-12) the substrate gap adjusting layer can be formed in zigzag pattern, so that the gap between the two substrates securely become equal in a wider area. Therefore, the first conductive layer has a zigzag shape with substantially

equal width of the sealing material to achieve a securely uniform thickness of the liquid crystal layer as claimed in claim 15 would have been obvious.

Claim 16, examiner's understanding a pitch of the first conductive layer is substantially equal to a pitch of the pixel electrode, and that is a inherent result to obtain a display area. So that a pitch of the conductive layer is equal to a pitch of the pixel electrode as claimed in claim 16 would have been obvious.

Claim 17 concerning the forming method for the first conductive layer is a product-by-process claim, which does not define a materially different invention, as there would be no way to tell by the product would have been used to make it, and therefore a product made by the process would not be patentably distinct from another with all of the limitations excepting the process limitations (see MPEP 2113).

***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (703)308-6213 .

Mike Qi
November 14, 2000

***Kenneth Parker***
***Primary Examiner***
***Technology Center 2800***